WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a memory cell array comprising a plurality of cells;

a plurality of sense amplifiers coupled to respective bit lines and respective bit-bar lines of respective cells in the plurality of cells, each of the plurality of sense amplifiers having a first terminal and a second terminal;

a control signal generating circuit to generate first, second, and third control signals;

a first switch to selectively couple the first terminals of the plurality of sense amplifiers to a power supply voltage terminal in response to the first control signal;

a second switch to selectively couple the second terminals of the plurality of sense amplifiers to a ground voltage terminal in response to the second control signal;

a third switch to selectively couple the first terminals of the plurality of sense amplifiers to a first charge recycling store in response to the third control signal; and

a fourth switch to selectively couple the second terminals of the plurality of sense amplifiers to a second charge recycling store in response to the third control signal.

2. A semiconductor memory device as defined in claim 1, wherein the first switch comprises a PMOS transistor having a gate coupled to

receive the first control signal, and the second switch comprises a NMOS transistor having a gate coupled to receive the second control signal.

3. A semiconductor memory device as defined in claim 1, wherein the control signal generating circuit comprises:

a first inverter circuit to selectively invert a bit line enable signal in response to a bit line precharge signal;

a latch coupled to receive an output of the first inverter circuit;

a delay circuit, coupled to receive an output of the latch, to generate the first control signal;

an inverting and delaying circuit, coupled to receive the output the latch, to generate the second control signal;

a pulse generating circuit to generate a pulse output based on the output of the latch;

a first logic circuit to generate an output based on a plurality of word line enable address signals;

a second inverter circuit to selectively invert the bit line enable signal in response to an output of the first logic circuit; and

a second logic circuit to generate the third control signal based on the pulse output and an output of the second inverter circuit.

4. A semiconductor memory device as defined in claim 3, wherein the first logic circuit comprises a NOR gate.

5. A semiconductor memory device as defined in claim 3, wherein the second logic circuit comprises a NOR gate.

6. A semiconductor memory device as defined in claim 1, wherein the first charge recycling store comprises a first capacitor, and wherein the second charge recycling store comprises a second capacitor.

7. A semiconductor memory device as defined in claim 1, further comprising:

a PMOS transistor coupled between a power supply terminal and the first charge recycling store, the PMOS transistor having a gate coupled to receive a power-up signal; and

a NMOS transistor coupled between the second charge recycling store and a ground terminal, the NMOS transistor having a gate coupled to receive the power-up signal.

8. A semiconductor memory device as defined in claim 1, wherein the third switch comprises a first transfer gate, and wherein the fourth switch comprises a second transfer gate.